UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
08/966,954	11/10/1997	JOHANNES R. GERARDUS DE VRIES	6211P001	6312

7590 06/13/2006

Jordan M. Becker
Blakely, Sokoloff, Taylor & Zafman LLP
12400 Wilshire Boulevard, Seventh Floor
Los Angeles, CA 90025-1030

EXAMINER	
PETRANEK, JACOB ANDREW	
ART UNIT	PAPER NUMBER
2183	

DATE MAILED: 06/13/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	08/966,954	GERARDUS DE VRIES, JOHANNES R.	
	Examiner	Art Unit	
	Jacob Petranek	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 April 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *44-47,49 and 50* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *44-47,49 and 50* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *4/14/1995* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 44-47 and 49-50 are pending.

2. The office acknowledges the following papers:

Specification, claims, IDS, arguments, and abstract filed on 4/18/2006.

IDS filed on 1/11/2006.

Notice of non-compliance

3. Claim 45 is currently non-compliant. The status identifier should be changed in the next correspondent.

Withdrawn objections

4. The drawing objection has been withdrawn.

5. The specification objections have been withdrawn.

6. The 35 USC § 112 second paragraph rejections for claims 46-47 and 49-50.

7. The 35 USC § 102b rejections of claims 46-47 under Chuang are withdrawn due to clarification of the claimed limitations.

New Claim Rejections - 35 USC § 112

8. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

9. Claims 44-47 and 49-50 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The limitation from claim 44 "A second assembly code level which includes a plurality of instructions which are accessible to the programmer and which can explicitly reference individual outputs of any of the plurality of functional units" is not contained within the specification upon a cursory glance. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

10. Claims 45-47 and 49-50 are rejected due to their dependency.

New Claim Rejections - 35 USC § 103

11. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

12. Claims 44-45 and 49-50 are rejected under 35 U.S.C. §103(a) as being unpatentable over Chuang (U.S. 4,766,566), in view of Labrousse et al. (U.S. 5,313,551).

13. As per claim 44:

Chuang disclosed a processor comprising:

A plurality of functional units coupled to each other to execute operations defined

from an instruction set of the processor (Chuang: Figure 7 elements 24, 60, 62, and 70, column 10 lines 18-41), the plurality of functional units including an arithmetic logic unit (ALU) and a multiplier (Chuang: Figure 7 elements 24, 60, 62, and 70, column 10 lines 18-41), the instruction set having a hierarchy of instruction levels, each of which can be used by a programmer to define instructions for the processor, the hierarchy of instruction levels including:

A RISC/CISC assembly code level (Chuang: Figure 7, column 5 lines 3-20)(The processor of figure 7 executes RISC instructions.), and

Chuang failed to teach a second assembly code level which includes a plurality of instructions which are accessible to the programmer and which can explicitly reference individual outputs of any of the plurality of functional units.

However, Labrousse disclosed a second assembly code level which includes a plurality of instructions which are accessible to the programmer and which can explicitly reference individual outputs of any of the plurality of functional units (Labrousse: Column 13 lines 35-42 and column 14 lines 17-22)(The instructions that contain bypass encoding signals are available to the programmer and are implemented into the instructions upon being compiled. Labrousse disclosed instructions that can be encoded with a bypass signal that can be used to bypass register reads without having a make a comparison between addresses for instructions.).

The advantage of encoding bypass signals within an instruction is that it will save the time needed to make comparisons between source registers between instructions and it will save space on the processor, which will lower costs (Labrousse: Column 2

lines 56-62). Allowing for bypass in the instruction will also result in the register value being available sooner to the instruction needing it, which may increase performance if the register access is in the critical path (Labrousse: Column 1 lines 49-64). The advantages of saving processor space and power, as well as increased performance would have motivated one of ordinary skill in the art to implement directly encoding bypass signals into instructions to execute. Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention to implement encoding bypass signals into instructions for the advantages of increased performance and decreased costs.

14. As per claim 45:

Chuang and Labrousse disclosed a processor as recited in claim 44, wherein the second assembly code level comprises a native machine language of the processor (Labrousse: Column 13 lines 35-42 and column 14 lines 17-22)(The instructions that contain bypass encoding signals are available to the programmer and are implemented into the instructions upon being compiled. Labrousse disclosed instructions that can be encoded with a bypass signal that can be used to bypass register reads without having a make a comparison between addresses for instructions. The instructions are inherently native to the processor upon the combination and can be used by the processor.).

15. As per claim 49:

Chuang and Labrousse disclosed a processor as recited in claim 44, further comprising:

A plurality of dedicated output buses, one for each of the functional units

(Chuang: Figure 7 element 63, column 10 lines 18-41)(Each functionality unit has an output bus to put the data on.); and

A plurality of bus registers, each coupled to store the output of only a corresponding one of the plurality of functional units and each coupled to only a corresponding one of the plurality of dedicated output buses (Chuang: Figure 7 element 68, column 10 lines 18-41)(The output registers are coupled to the functional units and the output buses. Thus having the same functionality.).

16. As per claim 50:

Chuang and Labrousse disclosed a processor as recited in claim 49, wherein each of the dedicated output buses is coupled to an input of at least one other of the plurality of functional units (Chuang: Figure 7 elements 17 and 56, column 10 lines 18-41)(The bus lines are coupled to the inputs of the functional units through the register file.).

17. Claims 44 and 46-47 are rejected under 35 U.S.C. §103(a) as being unpatentable over Simpson et al. (U.S. 5,487,022), in view of Labrousse et al. (U.S. 5,313,551).

18. As per claim 44:

Simpson disclosed a processor comprising:

A plurality of functional units coupled to each other to execute operations defined from an instruction set of the processor (Simpson: Figure 12 elements 210 and 220, column 20 lines 22-41), the plurality of functional units including an arithmetic logic unit

(ALU) and a multiplier (Simpson: Figure 3 elements 108 and 101; Figure 12 elements 210 and 220, column 20 lines 22-41), the instruction set having a hierarchy of instruction levels, each of which can be used by a programmer to define instructions for the processor, the hierarchy of instruction levels including:

A RISC/CISC assembly code level (Simpson: Figure 3, column 11 lines 1-16)(The processor of figure 3 executes RISC instructions.), and

Simpson failed to teach a second assembly code level which includes a plurality of instructions which are accessible to the programmer and which can explicitly reference individual outputs of any of the plurality of functional units.

However, Labrousse disclosed a second assembly code level which includes a plurality of instructions which are accessible to the programmer and which can explicitly reference individual outputs of any of the plurality of functional units (Labrousse: Column 13 lines 35-42 and column 14 lines 17-22)(The instructions that contain bypass encoding signals are available to the programmer and are implemented into the instructions upon being compiled. Labrousse disclosed instructions that can be encoded with a bypass signal that can be used to bypass register reads without having a make a comparison between addresses for instructions.).

The advantage of encoding bypass signals within an instruction is that it will save the time needed to make comparisons between source registers between instructions and it will save space on the processor, which will lower costs (Labrousse: Column 2 lines 56-62). Allowing for bypass in the instruction will also result in the register value being available sooner to the instruction needing it, which may increase performance if

the register access is in the critical path (Labrousse: Column 1 lines 49-64). The advantages of saving processor space and power, as well as increased performance would have motivated one of ordinary skill in the art to implement directly encoding bypass signals into instructions to execute. Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention to implement encoding bypass signals into instructions for the advantages of increased performance and decreased costs.

19. As per claim 46:

Simpson and Labrousse disclosed a processor as recited in claim 44, wherein the plurality of hierarchical instruction levels further comprise a vector processing assembly code level (Simpson: Figures 17-27, columns 25-33)(The RISC instruction set contains vector instructions.).

20. As per claim 47:

Simpson and Labrousse disclosed a processor as recited in claim 46, further comprising a plurality of special use control registers, wherein the plurality of hierarchical instruction levels further comprise a level for using the special use control registers (Simpson: Figure 7, column 14 lines 50-67 continued to column 15 lines 1-48)(The processor uses control registers).

Response to Arguments

21. The arguments presented by Applicant in the response, received on 1/3/2006 are considered persuasive.

22. Applicant argues that "Simpson nor Chuang disclose a second assembly code level that includes a plurality of instructions accessible to the programmer and which can explicitly reference individual outputs of any of the plurality of functional units."

This argument is found to be persuasive for the following reason. Chuang disclosed no bypassing mechanism and therefore can't possibly read upon the newly claimed limitation for claim 44. Simpson disclosed a bypassing mechanism, but doesn't give support for allowing the programmer to explicitly reference these data values. A new ground of rejection has been given.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

The following is text cited from 37 CFR 1.111(c): In amending in reply to a rejection of claims in an application or patent under reexamination, the applicant or patent owner must clearly point out the patentable novelty which he or she thinks the claims present in view of the state of the art disclosed by the references cited or the objections made. The applicant or patent owner must also show how the amendments avoid such references or objections.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jacob Petranek whose telephone number is 571-272-5988. The examiner can normally be reached on M-F 8:00-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Jacob Petranek
Examiner
Art Unit 2183

EDDIE CHAN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100

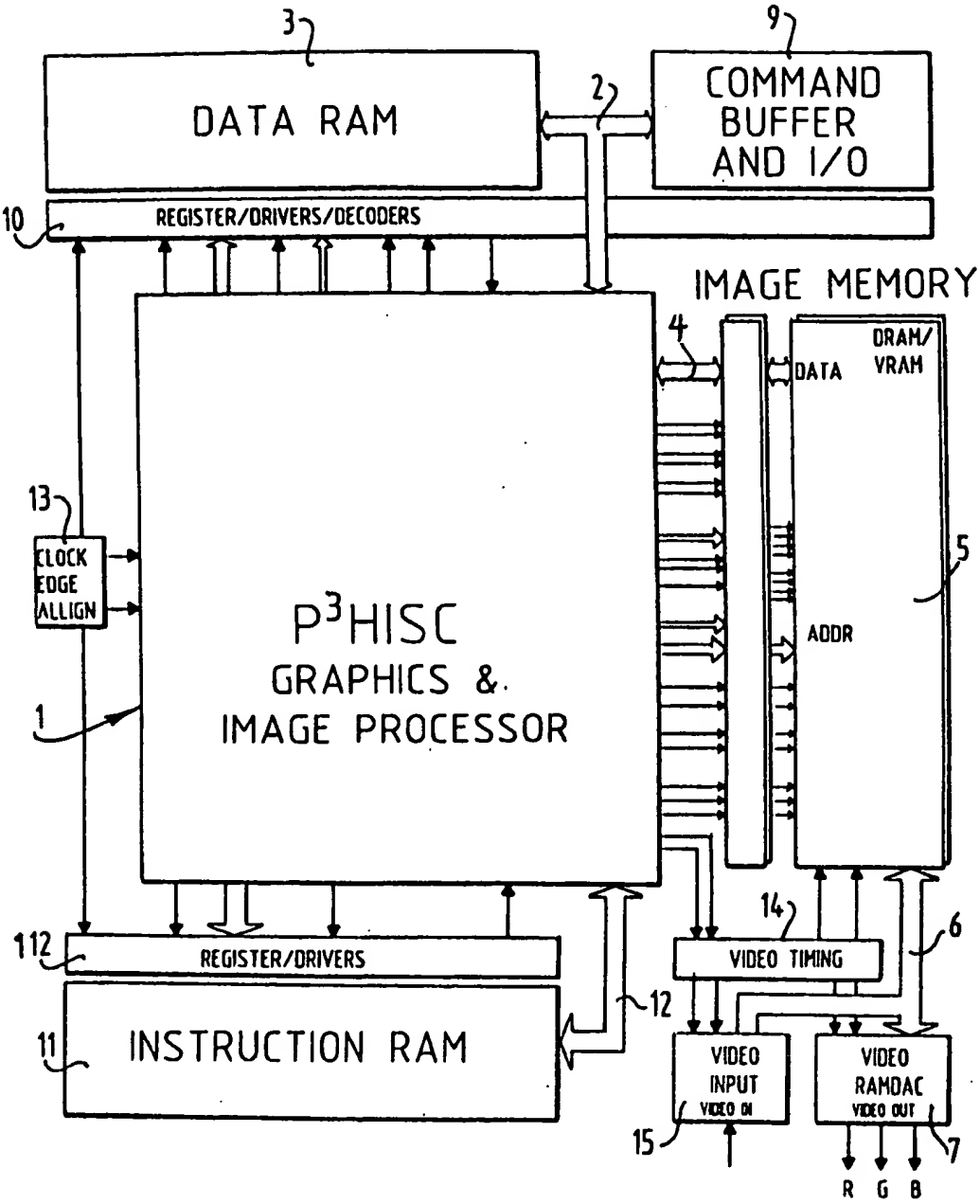

3
DATA RAM
9
COMMAND BUFFER AND I/O
2
10
REGISTER/DRIVERS/DECODERS
IMAGE MEMORY
4
DATA
DRAM/ VRAM
5
ADDR
13
CLOCK EDGE ALLIGN
P³HISC
GRAPHICS & IMAGE PROCESSOR
1
112
REGISTER/DRIVERS
14
VIDEO TIMING
6
12
11
INSTRUCTION RAM
VIDEO INPUT
VIDEO IN
VIDEO RAMDAC
VIDEO OUT
15
7
R G B

FIG.1

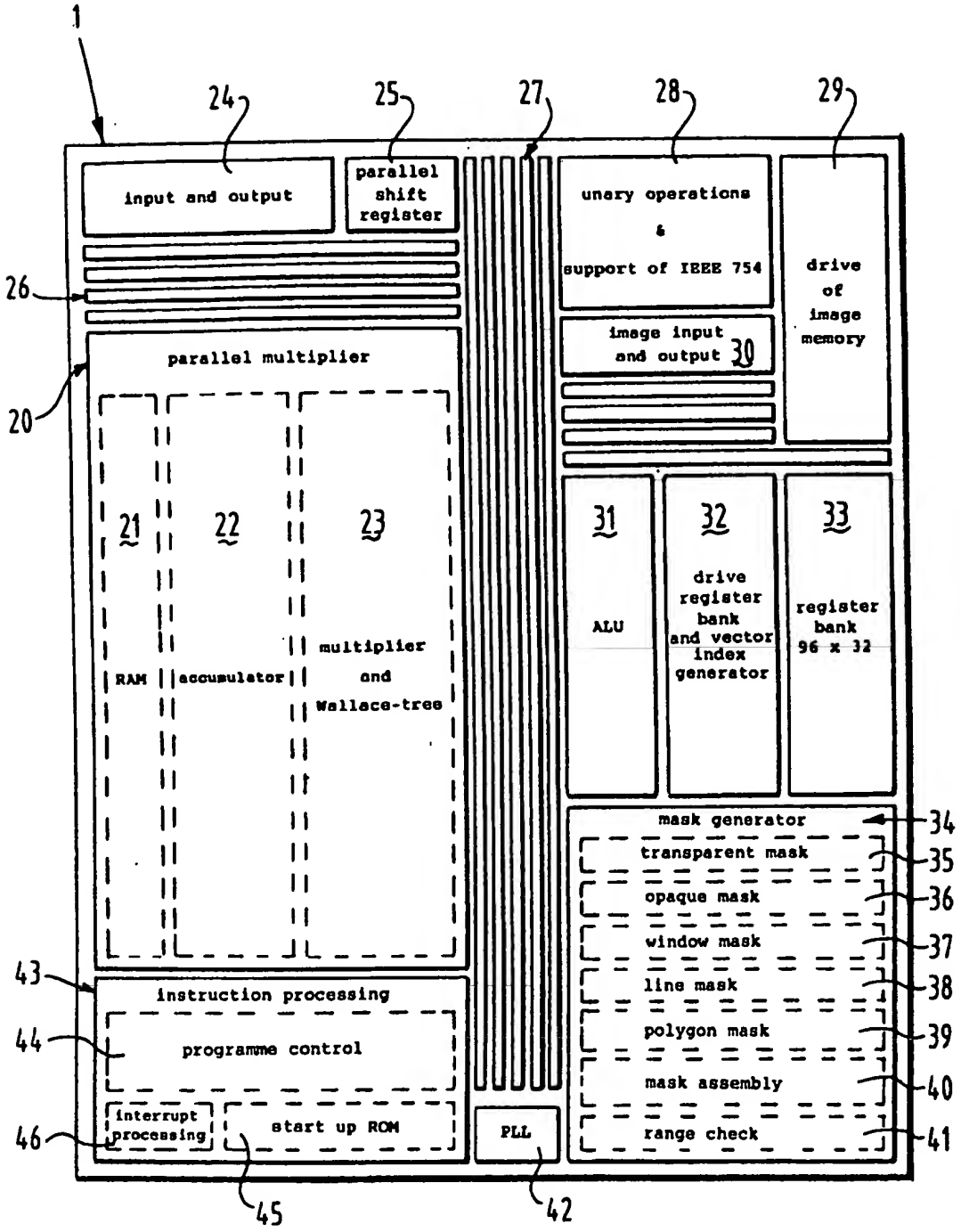

1
24
25
27
28
29
input and output
parallel shift register
unary operations & support of IEEE 754
drive of image memory
26
image input and output 30
parallel multiplier
20
21
22
23
RAM
accumulator
multiplier and Wallace-tree
31
ALU
32
drive register bank and vector index generator
33
register bank 96 x 32
mask generator
34
transparent mask
35
opaque mask
36
window mask
37
line mask
38
polygon mask
39
mask assembly
40
range check
41
43
instruction processing
44
programme control
interrupt processing
start up ROM
46
45
PLL
42

FIG. 2

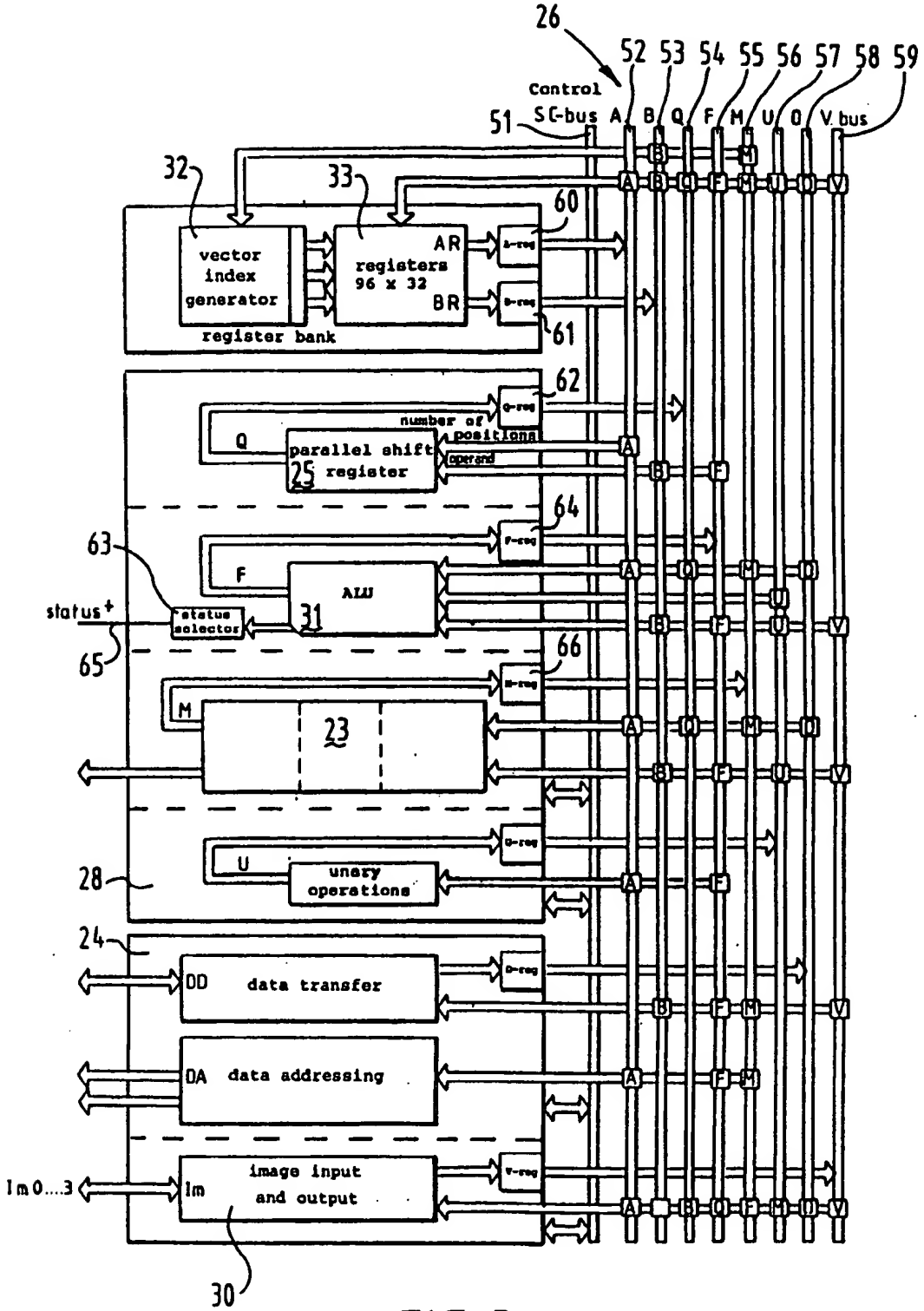
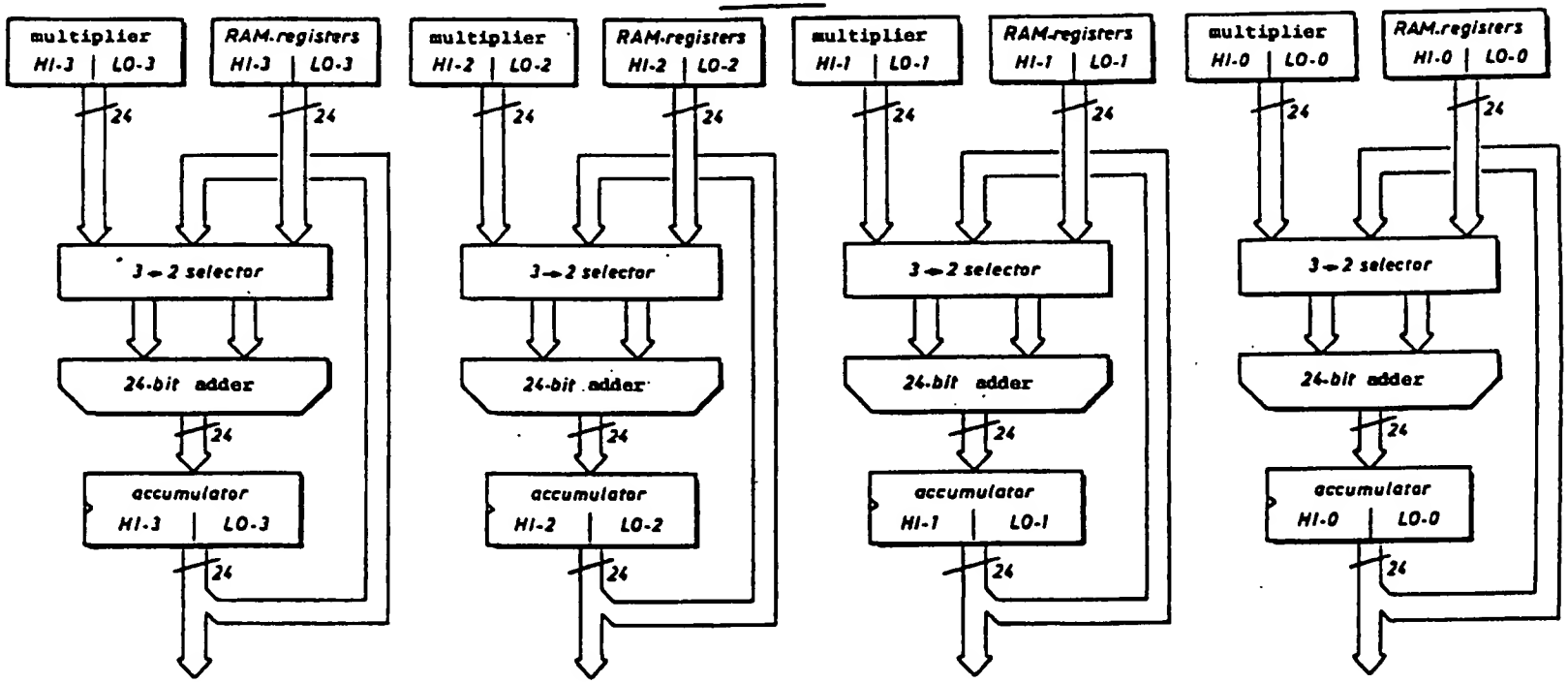

26
52
53
54
55
56
57
58
59
Control
SG-bus
A
B
Q
F
M
U
Q
V bus
51
32
33
60
vector index generator
registers 96 x 32
AR
BR
register bank
61
62
number of positions
Q
parallel shift register
operand
25
64
63
F
ALU
status
status selector
31
65
66
M
23
U
unary operations
28
24
OD
data transfer
OA
data addressing
Im 0....3
Im
image input and output
30

FIG. 3

FIG.4


multiplier
HI-3 | LO-3
RAM-registers
HI-3 | LO-3
multiplier
HI-2 | LO-2
RAM-registers
HI-2 | LO-2
multiplier
HI-1 | LO-1
RAM-registers
HI-1 | LO-1
multiplier
HI-0 | LO-0
RAM-registers
HI-0 | LO-0
24
3→2 selector
24-bit adder
accumulator
HI-3 | LO-3
accumulator
HI-2 | LO-2
accumulator
HI-1 | LO-1
accumulator
HI-0 | LO-0

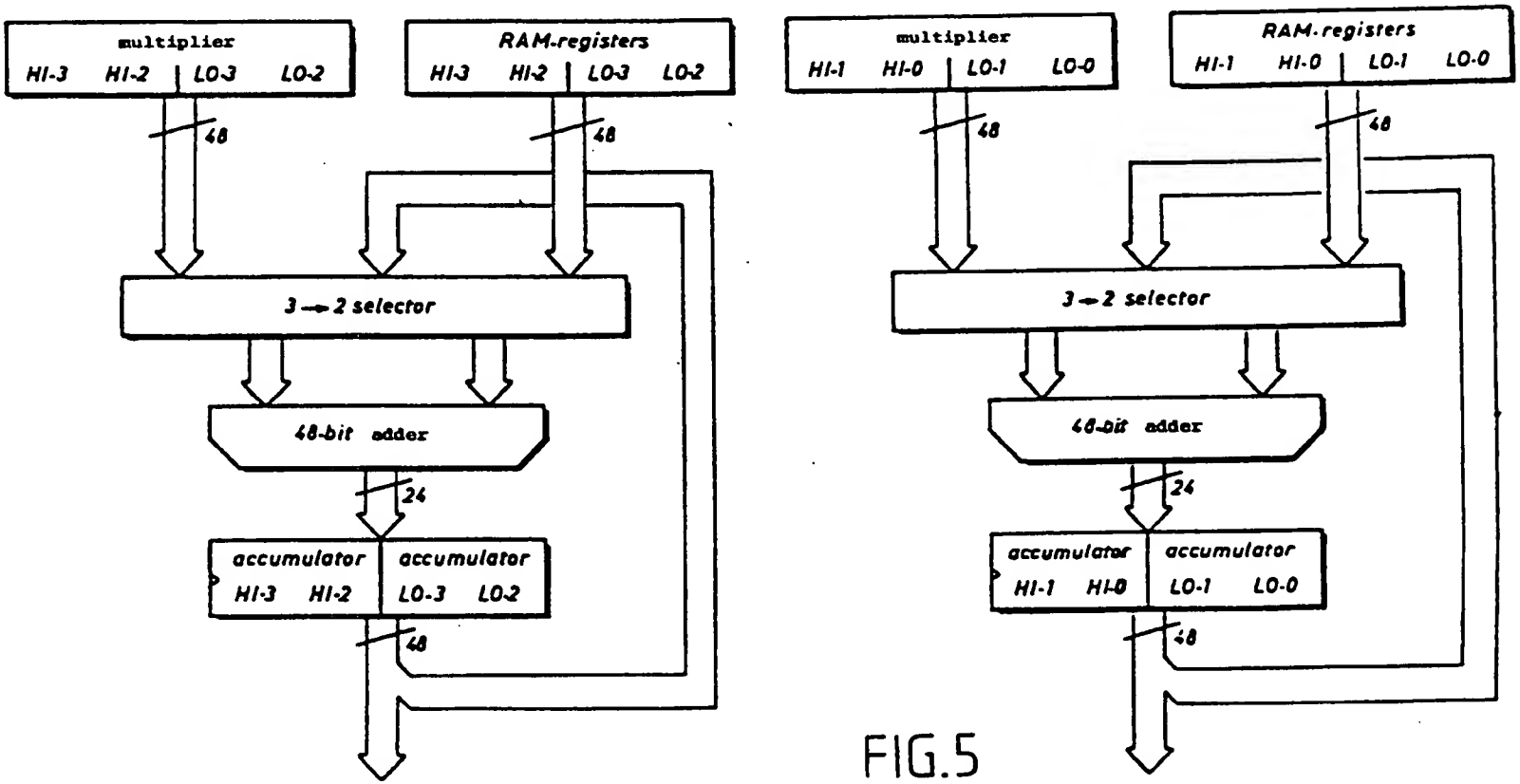

multiplier
HI-3 HI-2 LO-3 LO-2
RAM-registers
HI-3 HI-2 LO-3 LO-2
48
48
3 → 2 selector
48-bit adder
24
accumulator
HI-3 HI-2
accumulator
LO-3 LO-2
48
multiplier
HI-1 HI-0 LO-1 LO-0
RAM-registers
HI-1 HI-0 LO-1 LO-0
48
48
3 → 2 selector
48-bit adder
24
accumulator
HI-1 HI-0
accumulator
LO-1 LO-0
48

FIG.5

FIG.6

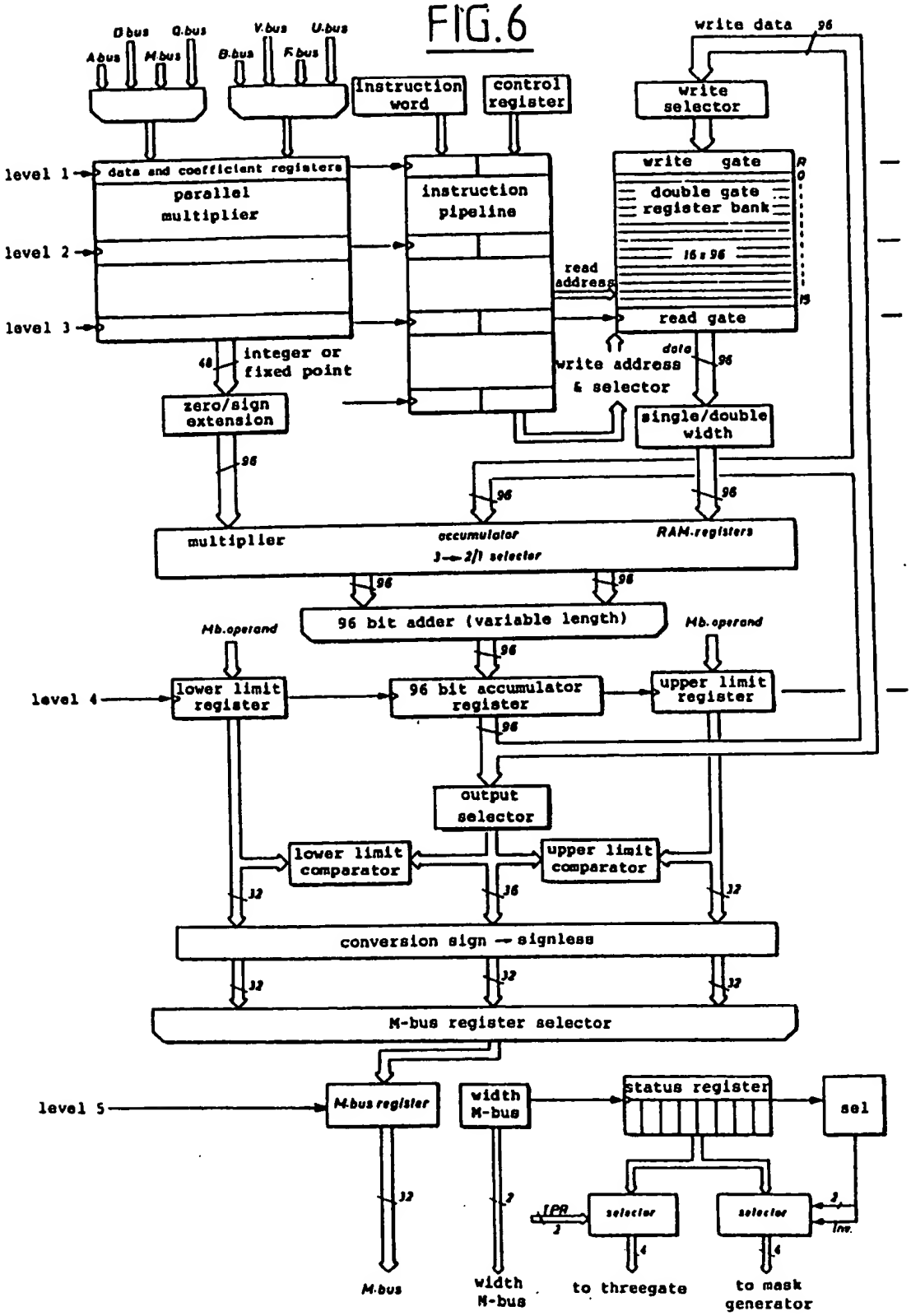
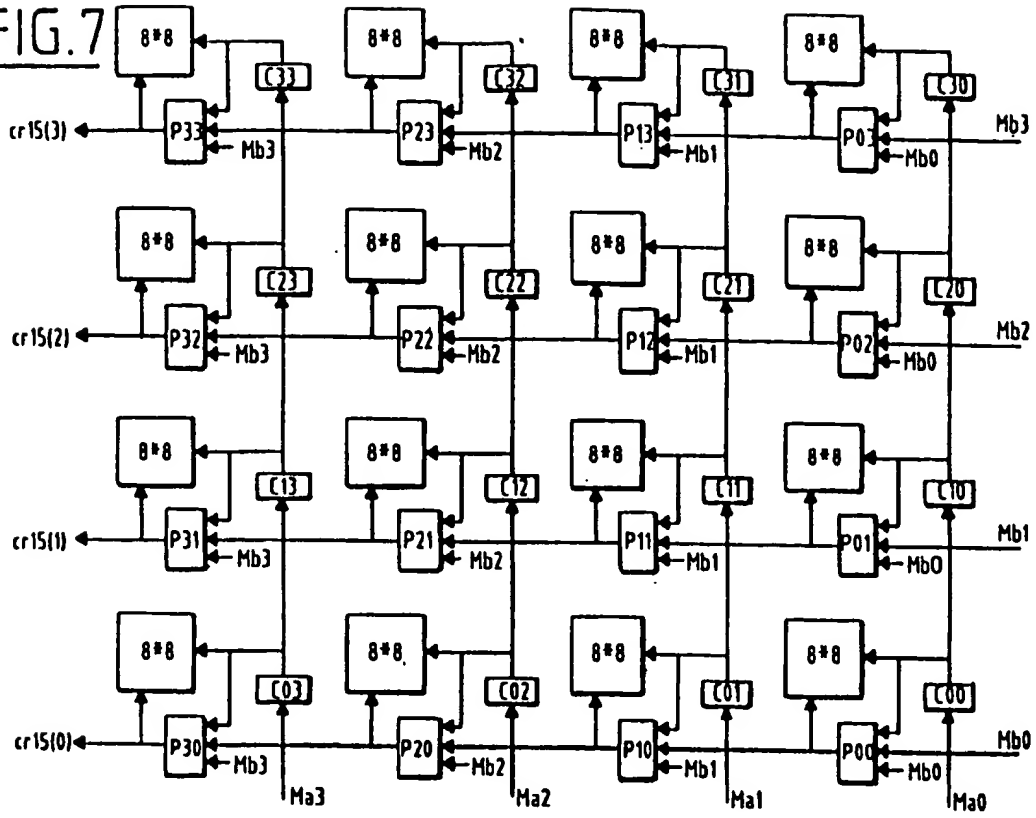

D bus
Q bus
V bus
U bus
A bus
M bus
B bus
F bus
instruction word
control register
write data
96
write selector
level 1
data and coefficient registers
parallel multiplier
level 2
level 3
instruction pipeline
write gate
double gate register bank
16 x 96
read address
read gate
data
write address & selector
integer or fixed point
zero/sign extension
single/double width
multiplier
accumulator
3 → 2/1 selector
RAM-registers
96 bit adder (variable length)
Mb.operand
level 4
lower limit register
96 bit accumulator register
upper limit register
output selector
lower limit comparator
upper limit comparator
conversion sign → signless
M-bus register selector
level 5
M.bus register
width M-bus
status register
sel
IPR
selector
to threegate
to mask generator
M.bus
width M-bus

FIG.7



16BIT MODE ROTATE+11 BIT

FIG.8 STAGE 1. FOUR 8 BIT ROTATES
STAGE 2. EIGHT 4 BIT 'CROSSES'